SPECIFICATION

PARALLEL PROCESSING DEVICE FOR GENERATING SHAPE AND/OR DISPLAYING IMAGE

TECHNOLOGICAL FIELD

The present invention relates to a more efficient and high speed processing device which creates and/or displays the a two dimensional (2D) shape and/or a three dimensional (3D) shape as an exclusive use or general purposes processing machine such as the shape generating process and the rendering process with the dynamic rendering technique, which are based on the organizing and/or structuring mechanism.

BACKGROUND ART

As a conventional 3D graphics machine, for example, many systems have been proposed such as CAPR of FUJITSU Co., Ltd., EXPRERT QA-2 which was developed by Kyoto University and LINKS-2 by Osaka University and MC of Matsushita Electric Industrial Co., Ltd., besides GT-5A of E&S Co. in the primacy. Still, as the goal of speed-up, the parallel processing mechanism in these machines is limited to the hidden plane process and/or the hidden line process and to the image displaying process by the ray tracing method, in other words "the ray tracing process."

Furthermore, as a typical example of the pipeline type machine, there are PROWERIRIS and INDIGO, etc. which are the exclusive machines developed by SGI Co. for processing the image. These machines are constituted by the geometric engine and the graphic engine and are made for the purpose of realizing an efficient time-varying image (including animatin) process, etc. The processing style of these systems is based on the modeling and rendering of the conventional methods, and these machine are fundamentally regarded as the specialized machine for displaying an image from the viewpoint of its original function.

The game machine "Nintendo 64" of Nintendo Co., Ltd. was developed based upon the pipeline system as a game machine. This is a high-performance machine which is

mounted on a 64 bit CPU as a system equal to the former machine of SGI.

However, in these prior arts, there are so many problems in which it is not possible to freely and easily construct the game generating environment, etc., because these prior art systems have been based on the conventional shape processing method.

The object of the present invention is to provide a parallel processing device for generating the shape and/or displaying the image which freely and easily constructs the game generating and/or executing environment and for realizing a communication tool in which a time-varying image process can be executed in multi-media.

DISCLOSURE OF THE INVENTION

The present invention relates to a device which carries out a sequential and/or simultaneous parallel process on the shape engine and/or the geometric engine and/or the graphic engine as a device creating and displaying a 3D shape and/or a 2D shape.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates one embodiment of the present invention, showing the PS1 which is a parallel processing device with the general process for generating the shape and/or displaying the image.

Fig. 2 shows the relationship between the vertex and the edge used in the above embodiment.

Fig. 3 is a block diagram of PS2 which is another embodiment of the parallel processing device for generating the shape and/or displaying the image; and

Fig. 4 is a block diagram of PS3 which is still another embodiment of the parallel processing device for generating the shape and/or displaying the image.

BEST MODE FOR CARRYING OUT THE INVENTION

Fig. 1 illustrates one embodiment of the present invention, showing the PS1 which is a parallel processing device with the general process for generating the shape and/or displaying the image.

The parallel processing device PS1 for generating the shape and/or displaying the image has a database system and/or the communication device C1, an image integrating processor PR0, a shape engine E1, a geometric engine E2, a graphic engine E3, memories

M1, M2, M3, and a screen control device DC.

The parallel processing device PS1 for generating the shape and/or displaying the image is hierarchically composed as a whole, and the image integrating processor PR0 is placed at the top (the highest position) of the hierarchy, and the processor PR0 unifies each of the engines E1, E2 and E3.

The shape engine E1 can generate the general shape naturally including the freely formed shape and realize freely and easily many changes and/or corrections of the target shape, etc. For example, based on the organizing and/or structuring mechanism, it deals with the required shape by making use of pointing devices, etc. as an auxiliary device in accordance with the drawing shape on a screen.

The shape engine E1 has an integrating processor PR1 for generating the target shape and displaying the image, a 1st arithmetic unit A11, a 2nd arithmetic unit A12, and a 3rd arithmetic unit A13. The integrating processor PR1 operates and controls the 1st arithmetic unit A11, the 2nd arithmetic unit A12, and the 3rd arithmetic unit A13.

The arithmetic units A11, A12 and A13 are operated and controlled respectively by the arithmetic mechanism corresponding with the vertex of a FACET, that is a hyperplane with a normal line (or merely called "normal"), which is formed as the triangular shape polygon of making the polyhedron, and the edge constituted according to these vertices of the FACET. Namely, for example, the 1st arithmetic unit A11 controls the calculating process with the 1st vertex and the 3rd edge of a predetermined triangle, the 2nd arithmetic unit A12 controls the calculating process with the 2nd vertex and the 2nd edge of the triangle, and the 3rd arithmetic unit A13 controls the calculating process with the 3rd vertex and the 1st edge of the triangle.

The 1st arithmetic unit A11 should control the calculating process with one vertex and one edge of the predetermined triangle, and it can control the calculating process with the combination except for the combination of the 1st vertex and the 3rd edge. Likewise, the 2nd arithmetic unit A12 and 3rd arithmetic unit A13 should control the calculating process with one vertex and one edge of the predetermined triangle, and they can control the calculating process with the combination except for the above combination.

The geometric engine E2 is an arithmetic unit which mainly converts the coordinate point equivalent to the vertex of FACET as the operation of transferring and/or rotating, etc., which is the process of the geometric conversion such as the coordinate point affected by the

transfer matrix. This process of the conversion is the arithmetic calculating process. The main object of the process is to carry out the shape displaying process on a screen dynamically.

The geometric engine E2 has an integrating processor PR2 for processing image conversion, a 1st arithmetic unit A21, a 2nd arithmetic unit A22 and a 3rd arithmetic unit A23. The integrating processor PR2 for processing the image conversion operates and controls the 1st arithmetic unit A21, the 2nd arithmetic unit A22 and the 3rd arithmetic unit A23. Each of the arithmetic units A21, A22 and A23 is operated and controlled as corresponding with the vertex of FACET and the edge constituted according to these vertices. Namely, for example, the 1st arithmetic unit A21 controls the process on the 1st vertex and the 3rd edge of the triangle, and the 2nd arithmetic unit A22 controls the process on the 2nd vertex and the 2nd edge of the triangle, and also the 3rd arithmetic unit A23 controls the process on the 3rd vertex and the 1st edge of the triangle.

Incidentally, the 1st arithmetic unit A21 should control one vertex and one edge of the triangle, and it can also control the combination except for the combination between the 1st vertex and the 3rd edge of the triangle. As to the 2nd arithmetic unit A22 and the 3rd arithmetic unit A23, each of them should control the process on one vertex and one edge of the triangle, and they can control the process on the combination except for the above-described combination. However, the 1st arithmetic unit A21 needs to correspond to the 1st arithmetic unit A11, the 2nd arithmetic unit A22 to the 2nd arithmetic unit A12, and also the 3rd arithmetic unit A23 to the 3rd arithmetic unit A13. In other words, for example, the 1st arithmetic unit A21 controls the process on the vertex and the edge equal to the vertex and the edge of the triangle which the 1st arithmetic unit A11 controls. The relation between the 2nd arithmetic unit A22 and the 2nd arithmetic unit A12 and the relation between the 3rd arithmetic unit A23 and the 3rd arithmetic unit A13 should be the same as that of the 1st arithmetic unit A21 and the 1st arithmetic unit A11.

More specifically, each arithmetic unit (what is called the calculating processor) A21, A 22, and A23 are connected directly to arithmetic units A11, A12, and A13 respectively as the forward stage corresponding through the pipeline PL. Therefore, positioning information of the vertex which constitutes the FACET can be processed by each arithmetic unit A21, A22, and A23 as shape data generated and/or changed by the arithmetic unit corresponding with the forward stage processing arithmetic unit A11, A12, and A13

respectively.

The graphic engine E3 mainly deals with a 3D shape and displays a 3D image and thus fulfills the roll of the rendering machine for the purpose of the hyper view and/or the hyper ray tracing process, that is the innovative rendering technique to do the dynamic rendering process. The rendering process is made as the result of being carried out by realizing the shape process based on the organizing and/or structuring mechanism

The graphic engine E3 has an integrating processor PR3 for processing the image display, a 1st arithmetic unit A31, a 2nd arithmetic unit A32, and a 3rd arithmetic unit A33. The integrating processor PR3 controls the 1st arithmetic unit A31, the 2nd arithmetic unit A32, and the 3rd arithmetic unit A33.

Each of the arithmetic unit A31, A32 and A33 is operated and controlled as corresponding with the vertex of FACET and the edge constituted according to these vertices. Namely, the 1st arithmetic unit A31, for example, controls the process on the 1st vertex and the 3rd edge of the triangle, the 2nd arithmetic unit A32 controls the calculating process with the 2nd vertex and the 2nd edge of the triangle, and the 3rd arithmetic unit A33 controls the calculating process with the 3rd vertex and the 1st edge of the triangle.

Incidentally, the 1st arithmetic unit A31 should control one vertex and one edge of the triangle, and it can also control the combination except for the combination between the 1st vertex and the 3rd edge of the triangle. As to the 2nd arithmetic unit A32 and the 3rd arithmetic unit A33, each of them should control the process on one vertex and one edge of the triangle, and they can control the process on the combination except for the above-described combination. However, the 1st arithmetic unit A31 needs to correspond to the 1st arithmetic unit A21, the 2nd arithmetic unit A32 to the 2nd arithmetic unit A22, and also the 3rd arithmetic unit A33 to the 3rd arithmetic unit A23. In other words, for example, the 1st arithmetic unit A31 controls the process on the vertex and the edge equal to the vertex and the edge of the triangle which the 1st arithmetic unit A21 controls. The relation between the 2nd arithmetic unit A32 and the 2nd arithmetic unit A22 and the relation between the 3rd arithmetic unit A33 and the 3rd arithmetic unit A23 should be the same as that of the 1st arithmetic unit A31 and the 1st arithmetic unit A21.

More specifically, each arithmetic unit (what is called the calculating processor) A31, A32, and A33 are connected directly to arithmetic units A21, A22, and A23 respectively as the forward stage corresponding through the pipeline PL.

Each arithmetic unit A31 and A32 and A33 respectively executes the luminosity calculation based on both coordinate data and normal line data of the FACET vertices, and constitutes displaying data of the 3D shape. These data made up as above are transferred to memory M3 for displaying the image, and then it is carried out to display the image on a displaying screen.

The solid line arrow in Fig. 1 indicates the flow between the control data and the shape data, and the bold solid line indicates pipelines PL in which the shape data can flow.

Each of the engines E1, E2 and E3 is set up as a tree type structure and/or a flat type structure. The arithmetic processing division of each of the engines E1, E2 and E3 is set up by three arithmetic units. Fundamentally, there is no interaction because of a freely and independently working processor, and thus each arithmetic unit can be constructed without the mutual control. The required control can be operated hierarchically by the inside processor for control in the calculating division.

The relation between vertices and edges used in the above embodiment is explained below.

Fig. 2 shows the relationship between vertices and edges used in this embodiment.

Fig. 2(1) shows such a condition that one given triangle is divided into four triangles, that is to say he 1st triangle T1, the 2nd triangle T2, the 3rd triangle T3, and the 4th triangle T4.

The 1st triangle T1 has the 1st vertex P11, the 2nd vertex P12, and the 3rd vertex P13, as well as the 1st edge SD11, the 2nd edge SD12, and the 3rd edge SD13.

The 2nd triangle T2 has the 1st vertex P21, the 2nd vertex P22, and the 3rd vertex P23, as well as the 1st edge SD21, the 2nd edge SD22, and the 3rd edge SD23.

The 3rd triangle T3 has the 1st vertex P31, the 2nd vertex P32, and the 3rd vertex P33, as well as the 1st edge SD31, the 2nd edge SD32, and the 3rd edge SD33.

The 4th triangle T4 has the 1st vertex P41, the 2nd vertex P42, and the 3rd vertex P43, as well as the 1st edge SD41, the 2nd edge SD42, and the 3rd edge SD43.

The operation and action of the embodiment will be described as follows.

First of all, in each engine of E1, E2 and E3, the 1st arithmetic unit executes the process on the 1st vertex and the 3rd edge of the FACET, and the second arithmetic unit does the process on the 2nd vertex and the 2nd edge, and the 3rd arithmetic unit does the process on the 3rd vertex and the 1st edge.

When the integrating processor PR1 is considered, the 1st arithmetic unit executes the process on the 1st vertex P11 and the 3rd edge SD13, the process on the 1st vertex P21 and the 3rd edge SD23, and the process on the 1st vertex P31 and the 3rd edge SD33, and the process on the 1st vertex P41 and the 3rd edge SD43. The 2nd arithmetic unit A12 executes the process on the 2nd vertex P12 and the 2nd edge SD12, the process on the 2nd vertex P22 and the 2nd edge SD22, the process on the 2nd vertex P32 and the 2nd edge SD32, and the process on the 2nd vertex P42, the 2nd edge SD42. The 3rd arithmetic unit A13 executes the process on the 3rd vertex P13 and the 1st edge SD11, the process on the 3rd vertex P23 and the 1st edge SD21, the process on the 3rd vertex P33 and the 1st edge SD31, and the process on the 3rd vertex P43 and the 1st edge SD41.

In both the integrating processor PR2 and PR3, as in the case of the processor PR1 as described above, the 1st arithmetic unit A21 executes the process on the 1st vertex and the 3rd edge, the 2nd arithmetic unit A22 does the process on the 2nd vertex and the 2nd edge, and the 3rd arithmetic unit A23 does the process on the 3rd vertex and the 1st edge.

The arithmetic process on points and lines is executed based on the vector operation. As a result, the shape composing point is generated and/or changed. As the arithmetic process is operated and/or controlled based on the organizing and/or structuring mechanism, the formed shape data are organized based on the above mechanism. Therefore, the control of the data flow of the pipeline PL is automatically realized based on the type of the above same mechanism.

The shape data which are created and/or changed here are transferred, through the pipeline PL shown by the bold solid line, to the geometric engine E2 and the graphic engine E3 one by one and processed.

The shape data which are created and/or changed at shape engine E1 and geometric engine E2 is transferred to graphic engine E3 by the same mechanism as described above. It can be designed that the shape data composed of shape engine E1 are directly transferred to graphic engine E3 and processed at graphic engine E3.

Each of the engines E1, E2 and E3 are connected by the pipeline PL so that the line-like and/or plane-like image are/is displayed. The control of these data flows is executed by processor PR0 which carries out the integration and management, and the environment of freely and easily drawn picture is constructed. In the above embodiment, so as to obtain the high speed and/or high quality picture image on a displaying screen, the data bus over 64 bits

is used to perform a quick operation.

The 64 bit composition (CPU) is adopted to the highway bus in each of arithmetic units from A12 to A33. The composition of the integrating and managing processors PR1, PR2 and PR3 adopts more than a 32 bit composition (CPU) level; and these processors are composed of exclusive CPU or custom IC.

Since the parallel processing device PS1 for generating the shape and/or displaying the image is realized as the processing machine for the freely formed shape, the shape engine E1 is mounted, and the composing device can be built up selectively for its required function while a unitary and consistent shape process is simultaneously possible; accordingly, the device of the present invention is the original and unique machine quite different from the mere displaying device developed until now. Clearly, the parallel processing device PS1 is the machine for freely and easily carrying out the 3D shape process, and the device is positioned as the exclusive machine which realizes the hyper view and/or the hyper ray tracing method based on the organizing and/or structuring mechanism.

Fig. 2(2) shows the condition wherein the triangle is divided at the generating level 2 in the above embodiment.

Here, the 1st triangle T1 is divided into triangles T5, T6, T7 and T8; the 2nd triangle T2 into triangles T9, T10, T11 and T12; the 3rd triangle T3 into triangles T13, T14, T15 and T16; and the 4th triangle T4 into triangles T17, T18, T19 and T20.

In the above embodiment, both whole and/or part management can be done by the basic processor PR0 which unifies the engine E1, E2 and E3 with the mechanism of monitoring the inside processors PR1, PR2 and PR3 which unifies the inside engines E1, E2 and E3.

Fig. 3 is a block diagram showing the parallel processing device PS2 for generating the shape and/or displaying the image, which is another embodiment of the present invention.

The inside processors PR1, PR2 and PR3, which have the roll of part management, are integrated by the parallel processing device PS2, and then the processing device PS2 is absorbed into the basic processor PR01. The basic processor PR01 has whole management and part management of them, thus being naturally referred to as only one device for executing the management and control.

Namely, the parallel processing device PS2 has the database and/or communication device C1, the image integrating processor PR01, the shape engine E11, the geometric engine

E21, the graphic engine E31 and the screen controlling device DC. The shape engine E11 has the 1st arithmetic unit A11, the 2nd arithmetic unit A12 and the 3rd arithmetic unit A13; the geometric engine E21 has the 1st arithmetic unit A21, the 2nd arithmetic unit A22 and the 3rd arithmetic unit A23; the graphic engine E31 has the 1st arithmetic unit A31, the 2nd arithmetic unit A32 and the 3rd arithmetic unit A33.

Required functions can be constructed by selectively combining each of the composed engines E1, E2 and E3 in this embodiment. In short, it is possible to construct the function of this embodiment by specifying the function of the basic processor PR0 and PR01, which fundamentally unifies the whole device, from the outside. The required function can be constructed by choosing circuit selection means in inside for establishing the composition against the device purpose and/or function.

Namely, the video game software is achieved by the shape engine E1, the geometric engine E2 and the graphic engine E3, like in a case of the parallel processing device PS1. It is also possible that the composition to enjoy the playing game is made by the geometric engine E2 and the graphic engine E3, without the shape engine E1 by removing it from the parallel processing device PS1.

In the above embodiment, the cascade combination (direct connection) of each engine E1, E2 and E3 is realized by the pipeline PL. The arithmetic processing part and/or the arithmetic processing unit which is constituted by each engine E1, E2 and E3 is connected directly through the pipeline PL. Also, the arithmetic unit in each of the engines E1, E2 and E3 is connected to each other by combining the arithmetic unit placed at each of the engines E1 and E2 and E3 one by one.

Under the condition for combining the two or three engines, the bypass line can be set up between the engines for a selection of the function. In other words, in the above embodiment, each engine E1 is directly connected to E2, and the engine E2 is directly connected to engine E3; however, a direct data transmission from engines E1 to E3 is also possible.

As a buffering function is given by the memory M1 provided between the inside processor PR1 and PR2 and by the memory M2 provided between the inside processors PR2 and PR3, it is possible to substitute the integrated function of the inside processors PR1, PR2 and PR3. Namely, if the processing speed of inside processor PR1 is more rapid than the processing speed of inside processor PR2, processing data are stored in memory M1; and if

the inside processor PR2 takes out the required data and deals with it as necessary, the inside processor PR1 does not need to consider the processing speed of the inside processor PR2. As seen from the above, it is possible to automatically solve the bottleneck of the data flow by installing memories, which has a buffering function, between the inside processors. The memory M2 works as in the same manner as the memory M1.

Incidentally, the pipeline PL can be provided between the memories M1 and M2 that have the buffering function.

In addition, the memories M1 and M2 can be omitted from the parallel processing device PS1, while the image integrating processor PR0 is designed so as to control and execute the function of the buffering referred to above.

Fig. 4 is a block diagram, showing the parallel processing device PS3, which is another embodiment of the present invention.

The parallel processing device PS3 has shape engines from $E1_1$ to $E1_{256}$ which are similar to the shape engine E1, geometric engines from $E2_1$ to $E2_{256}$ which are similar to the geometric engine E2, and graphic engine from $E3_1$ to $E3_{256}$ which are similar to the graphic engine E3. More specifically, 256 of the shape engines, the geometric engines, and the graphic engines are provided respectively, and the image integration processor PR02 controls these engines, respectively. Therefore, each of engines above has 4 n-th power (4^n) pieces. That is to say, each engine is respectively set up by 4^n pieces of sub engines, where **n** is a numerical number which shows the organizing composition level or the shape generating level of the curved surface body, and the minimum value of **n** is 0.

In addition, in the above embodiment, a basic configuration unit of one engine is set up by three pieces of the arithmetic unit.

The organizing and/or structuring mechanism and the dynamic rendering process works easily and efficiently to realize the process for generating the shape and/or displaying the image even in the usual calculating machine having a general purpose. The parallel processing device of the present invention works freely and efficiently as a super speed machine. Therefore, a comfortable and efficient communication environment can be realized in the mechanical communication as a will-transmission means. Thus, the parallel processing device of the present invention sufficiently satisfies many requirements for the multi-media environment.

Therefore, each embodiment works not only as a device of the desktop type but also

as a device of handy-type, becoming a free communication tool in the multi-media environment.

In this case, the communication by the usual screen can be used as a communication means in cyberspace; and virtual reality, etc. can be freely and efficiently realized as a tool of the more advanced communication environment. Moreover, as a means for constructing a comfortable game environment, it is possible to offer not only the game generating environment, which is constructing with efficiency and a low cost, but also the game executing environment.

The technology level of the embodiment of the present invention is so high that this technology will change the recent game generating and/or executing environment. A game of higher picture quality with respect to bi-direction games in the 3D world, etc. will be constructed by the technology of the present invention. Therefore, against not only more real games but also advanced simulation about various environments and analyses of objects, the effective evaluation system can be constructed. By the present invention, more effective CAD systems and training devices, etc. are also constructed.